Claims

1-24 Canceled

25. (New) A Method of improving immunity to interference of an integrated circuit (16), the method comprising:

transferring one or more error signals between at least one microprocessor chip or multiple processor µC (1) and at least one further component (2); and

defining, for the transferring of error signals, a minimum pulse length that is independent of a clock frequency of the microprocessor chip or the multiple processor is defined, starting from a signal on an error line having a defined pulse length is interpreted as an error.

26. (New) A method according to claim 25, wherein the further component is a mixed-signal module.

27. (New) A method according to claim 25, wherein in the event of a sequence of errors with a distance between the errors that is smaller than the minimum pulse length, the time of the sequence of errors output over the at least one error line is extended with respect to the actual error sequence time.

28. (New) A method according to claim 25, wherein the error signal in a chip, which receives the error signal of another chip or component, are not processed when the signals do not reach a minimum duration, and are processed when the minimum duration is reached or exceeded, and the signals are directed through at least one filter.

29. (New) A method according to claim 25, wherein at least one watchdog time window

(17) is predetermined in the integrated circuit or in the further component (2), within which at least one artificially produced error signal or error signal pattern is generated and tested so that the error detection circuits become self-testable.

30. (New) A method according to claim 29, wherein the watchdog time window (17) has a delay time TWindowDelay, and the time window, in which at least one error signal or error signal pattern is expected, remains open until the expiry of the delay time TWindowDelay.

31. (New) A method according to claim 30, wherein the delay time TWindowDelay is longer than the filter time TFilter of the filter(s) (7, 7') processing the error signal or error signals of the at least one error line (3, 3').

32. (New) A method according to claim 30, wherein the time window TWindowDelay is set in the further component (2) by way of the interface (5) connected to chip (1).

33. (New) A method according to claim 30, wherein a condition TWindowDelay is satisfied in excess of the filter time TFilter.

34. (New) A method according to claim 30, wherein the delay TWindowDelay approximately corresponds to twice the time TFilter.

35. (New) A method according to claim 25, wherein inside the chip (1) that sends error signals, the error signals are extended and/or output with delay one after the other through the error line.

36. (New) A method according to claim 25, wherein a test of the at least one error line (3, 4) is performed with the aid of an interface (5).

37. (New) A method according to claim 25, wherein the error signals are filtered by filters (7, 7') with a defined filter time TFilter.

38. (New) A method according to claim 25, wherein the pulse width TMin is set to a value of at least 30 nanoseconds approximately.

39. (New) An integrated circuit comprising:

at least one microprocessor chip or multiple processor microcontroller (1) or microprocessor module;

at least one additional separate component (2) having separately arranged power elements; and

one or more pulse extending devices or signal delaying devices for outputting error pulses (6, 6') one after another through at least one error line (3, 4).

40. (New) An integrated circuit according to claim 39 further comprising: one or more filters (7, 7') for filtering the error signals transferred through the error lines (3, 4).

41. (New) An integrated circuit comprising:

at least one microprocessor chip or multiple processor microcontroller (1);

at least one additional component (2) having separately arranged power elements, wherein one or more error signal is transferred between the at least one microprocessor chip or multiple processor µC (1) and the at least one additional component (2); and

one or more filter (7, 7') for filtering error pulses (6, 6') through at least one error line (3, 4).

42. (New) An integrated circuit according to claim 41, wherein the filter (7, 7') is configured as a digital forward/backward counter.

43. (New) An integrated circuit according to claim 41, wherein the chips or components are interconnected by at least one bus (5) and at least one error line (3, 4).

44. (New) An integrated circuit according to claim 43, wherein the circuit includes hardware test structures, with the aid of which a test of the at least one error line (3, 4) can be performed using an interface (5).

45. (New) An integrated circuit according to claim 41, wherein the microprocessor chip (1) or the additional component comprises at least one watchdog window circuit (50).

46. (New) An integrated circuit according to claim 45, wherein the watchdog window circuit (50) predefines a watchdog time window (17), and the watchdog time window (17) has a delay time TWindowDelay, and the time window, in which at least one error signal or error signal pattern is expected, remains open until the expiry of the delay time TWindowDelay.

47. (New) An integrated circuit according to claim 45, wherein the delay time TWindowDelay is longer than the filter time TFilter of the filter(s) (7, 7') processing the error signal(s) of the at least one error line (3, 3').